IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Pete D. Vogt
Serial No.:	10/714,026
Examiner:	John J. Tabone, Jr.
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Group Art Unit:	2138
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For:	LANE TESTING WITH VARIABLE MAPPING
Date:	May 14, 2007

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APPEAL BRIEF

This Appeal Brief is in furtherance of the Notice of Appeal filed March 13, 2007.

Applicant appeals the final rejection of claims 2-5, 7, 12 and 17.

REAL PARTY IN INTEREST

The present application has been assigned to the following party:

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RELATED APPEALS AND INTERFERENCES

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the Applicant's legal representative.

STATUS OF CLAIMS

Claims pending in the application: 1-9 and 11-34.

Claims allowed: 19-27.

Claims canceled: 10.

Claims rejected: 1-9, 11-18, and 28-34.

Claims appealed: 2-5, 7, 12, and 17.

STATUS OF AMENDMENTS

An Amendment After Final Rejection was filed on February 20, 2007 but not entered by the Examiner, as indicated in the Advisory Action mailed March 23, 2007. The claims, therefore, remain as amended in an earlier Response filed on August 30, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 (from which appealed claims 2-5 and 7 depend) is drawn to a memory agent including a receive link interface, a transmit link interface, and a loop back unit coupled to the receive link interface and a transmit link interface. An example embodiment of such a memory agent is illustrated in Fig. 32 and described in the substitute specification at page 35, lines 5-13. The loop back unit may selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation (for example, see substitute specification, page 35, lines 10-16).

Claim 2 depends from claim 1 and is drawn to the memory agent of claim 1, further including a second transmit link interface having a plurality of second transmit links and a second receive link interface having a plurality of second receive links. Exemplary embodiments of the recited limitations are shown, for example, in Figure 24, where the inner port 136 of the memory agent 134 includes a receive and a transmit link interfaces 140 and 142 respectively, and lanes in the links 54A and 56B implement the recited first receive lanes and first transmit lanes respectively. And the outer port 138 includes second receive and second transmit link interfaces 144 and 146 respectively, and lanes in the links 56A and 56B implement the recited second receive lanes and second transmit lanes respectively.

Claim 3 depends from claim 2 and recites a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the

second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface. Such a passthrough mode is disclosed in the substitute specification, for example, at page 36, lines 9-13.

Claim 4 depends from claim 1 and recites that the memory agent may selectively map one of the receive lanes to more than one of the transmit lanes during a lane testing operation. Thus, in an exemplary embodiment such as that disclosed in Figure 32 (page 32, lines 2-5), a training sequence may make a round trip from a memory controller to the memory agent, through a loopback unit in the memory agent (as recited in claim 1), and then back to the memory controller. The loopback unit 196 of Figure 32 may selectively map one of the receive lanes (incoming lanes coupled to the receive link interface 140) to more than one of the transmit lanes (outgoing lanes coupled to the transmit link interface 142) during a lane testing operation. Note that the recited selective mapping occurs inside the memory agent 134 of Figure 32 and is performed by the loopback unit.

Claim 5 depends from claim 1 and recites that the memory agent may selectively map one or more of the first receive lanes to one or more of the second transmit lanes according to a plurality of mappings. Figure 32 discloses an exemplary embodiment of a memory agent with receive lanes mapped to transmit lanes according to a plurality of mapping disclosed, for example, in Figure 33.

Claim 7 depends from claim 1 and recites that the memory agent may retransmit the received training sequence with modification as the return sequence. As disclosed in the substitute specification, for example, the memory agent may retransmit most of the training sequence as the return sequence while modifying only a small group within the sequence to provide identifying or status information to the memory host (substitute specification, page 36, lines 9-13).

Claim 12 is drawn to a memory agent comprising a first link interface having a plurality of first lanes and a second link interface having a plurality of second lanes. In one embodiment, the memory agent may be a memory controller. The memory agent may transmit training sequences having different mapping indicators to one or more of the plurality of first lanes, as disclosed in the substitute specification, page 35, lines 28-29. The memory agent may receive and analyze the return sequence to identify failed bit lanes, as disclosed in the substitute specification at page 35, lines 15-17.

Claim 17 depends from claim 17 and recites a memory agent transmitting electrical stress patterns in the training sequences. Such electrical stress pattern is disclosed, for example, in the substitute specification at page 30, lines 28-30 and page 31, lines 1-3.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 12 and 17 are unpatentable under 35 U.S.C. 102(e) as being anticipated by Bunton et al. (U.S. Patent No. 6,961,347).

Whether claims 2-5 and 7 are unpatentable under 35 U.S.C. 103(a) as being obvious over Bunton in view of Li et al. (U.S. Patent No. 5,515,361).

ARGUMENT

Rejections under 35 USC §102

Claims 12, 17 are rejected under 35 USC §102(e) as being anticipated by Bunton.

Claim 12

Claim 12 recites that the memory agent may *analyze the return sequences to identify failed lanes in the plurality of the first lanes and the plurality of second lanes*. Support for this limitation maybe found in the substitute specification, e.g., at page 32, lines 5-9. For example, the memory controller 50 of Figure 6 may be the recited memory agent, the multiple lanes in the outbound link 54 may be the recited first lanes (through which the memory controller 50 transmits training sequence to the memory modules 52), the multiple lanes in the inbound link 56 may be the recited second lanes (through which the memory controller 50 receives return sequences from the memory modules 52), and the memory controller 50 may analyze the return sequences to identify failed lanes in the plurality of first lanes (outbound link 54) and second lanes (inbound link 56). The Examiner does not specifically point out where Bunton discloses this limitation.

Bunton, in Figure 4, illustrates training Port A and Port B and discloses the following:

> "FIG. 4 represents a time line for both Port A 400 and Port B 410 with time elapsing toward the bottom of the figure. Before training begins, Port A 400 may exist in an enabled state 440 while Port B is in a disabled or link down state 450. By transmitting an initial sequence of TS1 training sets 420, Port A 400 can effectively wake up Port B 410 from a disabled state to an enabled state 440. Once Port B is enabled 440, two things occur. First, Port B 410 will begin transmitting TS1 training sets back to Port A 400. Secondly, Port B 410 will check the content

of the incoming TS1 training sets 420 to see if the data was received as it was sent. If there is any discrepancy, Port B 410 will correct the incoming signals so that the original content of TS1 420 is restored. At this point, Port B 410 will be trained 460 and will respond by sending the second training set, TS2 430, back to Port A 400.

Meanwhile, Port A 400 has been receiving TS1 data 420 from Port B 410 and performs the same signal integrity checks and correction that Port B has completed." (Bunton, column 7, lines 42-57, underlining added)

That is, Bunton's Port B checks the training sequence it receives from Port A to identify any possible error in the signal from Port A to Port B, and in the process, gets trained. Similarly, Port A checks the training sequence it receives from Port B to identify any possible error in the signal from Port B to Port A. Bunton, however, does not disclose any technique for analyzing the training sequence Port A receives from Port B to identify any possible error in the signal from Port A to Port B *and* in the signal from Port B to Port A. That is, to the extent Bunton may be interpreted as analyzing return sequences to identify failed lanes, the return sequences only enable Port A to identify misordered lanes in the second plurality of lanes, i.e., the lanes on which the return sequences are received from Port B to Port A. Bunton fails to disclose that Port A may analyze the return sequences to identify failed lanes in the lane from Port A to Port B *and* in the lane from Port B to Port A, as would be required by claim 12.

Additionally, claim 12 recites that the memory agent may transmit training sequences having different *mapping indicators on one or more of the plurality of first lanes*. As disclosed in the specification, a mapping indicator instructs the memory agent which mapping to use (substitute specification, page 35, lines 28-29). Exemplary embodiments of different mappings are illustrated in Fig. 33 (e.g., mapping A, mapping B). Although the Examiner alleges that Bunton's Figure 9 discloses mapping (Final office action dated 11/17/2006, page 3, last 2 lines), the Examiner fails to specifically point out where Bunton discloses the recited mapping indicator.

Bunton discloses transmitting training sequence in each lane of a multi lane link. The training sequence of each lane includes a unique lane identifier symbol (Bunton, column 4, lines 49-51). A receive port can determine the identity of a lane from the unique lane identifier of that lane (Bunton, column 10, lines 46-48). That is, the unique lane identifier may be used to identify a lane; however, the lane identifier does not instruct a memory agent which mapping to use. Even if *arguendo*, Bunton's Figure 9 disclose a mapping as alleged by the Examiner, Bunton

fails to disclose transmitting training sequences having *different mapping indicators* on one or more of the plurality of first lanes, where the mapping indicator indicates to the memory agent which mapping to use.

Claim 17

Claim 17 depends from claim 12 and recites a memory agent transmitting electrical stress patterns in the training sequences.

In rejecting claim 17, the Examiner makes the conclusory statement that Bunton teaches the memory agent may transmit electrical stress patterns in the training sequences with reference to the Abstract; col. 4, lines 18-54; col. 7, line 18 through col. 9, line 8; Figs. 4-6; col. 10, line 29 through col. 12, line 8; and Figs. 9-12. Bunton, however, fails to disclose any thing relating to electrical stress patterns, and the Examiner has failed to show how the cited sections would support such a conclusion.

Rejections under 35 USC §103

Claims 2-5 and 7 are rejected under 35 USC §103(a) as being anticipated by Bunton in view of Li.

Claim 2

Claim 1 (from which claim 2 depends) recites *a receive link interface having a plurality of receive lanes to receive training sequences; a transmit link interface having a plurality of transmit lanes to transmit return sequences.* Exemplary embodiments of the recited limitations are shown, for example, in Figure 24, where the inner port 136 of the memory agent 134 includes receive and a transmit link interfaces 140 and 142 respectively, and lanes in the links 54A and 56B implement the recited receive lanes and transmit lanes respectively. While rejecting claim 1, the Examiner appeared to allege that Bunton's HCA 220 of Figure 2 is the recited memory agent and the physical link 140 is the recited transmit lanes and the receive lanes. Bunton discloses that the physical link 140 may be a *two lane link*, where "data would flow through one lane in one direction while data would flow through the parallel lane the other direction." (Bunton, column 6, lines 61-63). That is, the Examiner appears to allege Bunton's two lanes of the physical link 140 disclose the recited transmit lanes and receive lanes of claim 1.

Claim 2 recites that the *memory agent according to claim 1 ... further comprising: a second transmit link interface having a plurality of second transmit lanes; and a second receive link interface having a plurality of second transmit lanes*. Exemplary embodiments of the recited limitations are shown, for example, in Fig. 24, where the outer port 138 includes a second receive and second transmit link interfaces 144 and 146 respectively, and lanes in the links 56A and 56B implement the recited second receive lanes and second transmit lanes respectively. The Examiner alleges that Bunton discloses this limitation and points to Bunton's physical link 140 coupled to the HCA 220.

Bunton's HCA 220 is coupled to the physical link 140 and the Host bus (see Figure 2). As discussed above, the Examiner had earlier alleged that the two lanes of the physical link 140 are the recited receive lanes and transmit lanes of claim 1. The physical link 140, hence, can not be the recited *second transmit lanes* and the *second transmit lanes* of claim 2. Moreover, Bunton fails to disclose that the Host Bus includes a separate *second transmit lanes* and the *second transmit lanes*. Additionally, Bunton fails to disclose the recited *second transmit link interface* and the *second receive link interface*. Thus, the references do not disclose all the elements recited in claim 2, and the Examiner has not set forth a reason to modify the references to include all the limitations of claim 2. A *prima facie* case of obviousness, therefore, has not been established with respect to claim 2.

Claim 3

Claim 1 recites that *the memory agent may operate in a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface.*

The Examiner acknowledges that Bunton does not teach the recited loop back unit of claim 1 (from which claim 3 depends) but alleges that Li teaches such a loop back unit. The Examiner further acknowledges that Li teaches that "in the normal mode of operation of the loopback switch 301, optical switch 208 is set in the 'bar' position 302" (Final office action, dated 11/17/2006, page 8, lines 5-6, underline added), which the Examiner alleges discloses the recited passthrough mode. That is, to the extent Li's 'bar' position 302 discloses the recited passthrough mode, the 'bar' position 302 is enabled during the normal mode of operation, as has

been acknowledged by the Examiner. In contrast, claim 3 recites a *passthrough mode* during a *lane testing operation*, which Li fails to disclose. Thus, the references do not disclose all the elements recited in claim 3, and the Examiner has not set forth a reason to modify the references to include all the limitations of claim 3. A *prima facie* case of obviousness, therefore, has not been established with respect to claim 3.

Claim 4

Claim 4 recites that *the memory agent may selectively map one of the receive lanes to more than one of the transmit lanes during a lane testing operation*. Thus, in an embodiment such as that disclosed in Figure 32 (page 32, lines 2-5), a training sequence may make a round trip from a memory controller to the memory agent, through a loopback unit in the memory agent (as recited in claim 1), and then back to the memory controller. The *loopback unit* 196 of Figure 32 may selectively map one of the receive lanes (incoming lanes coupled to the receive link interface 140) to more than one of the transmit lanes (outgoing lanes coupled to the transmit link interface 142) during a lane testing operation. Note that the recited selective mapping occurs inside the memory agent 134 of Figure 32 and is performed by the loopback unit.

The Examiner, while rejecting claim 1, acknowledges that Bunton does not teach a loopback unit (Final office action, dated 11/17/2006, page 7, line 1). While rejecting claim 4, the Examiner appears to allege that Bunton's Figures 4-6 and 9-12 disclose the recited limitation.

In Figure 4, Bunton discloses that Port B 410 may transmit TS1 training sequence back to Port A 400 (Bunton, column 7, lines 49-50). Bunton, however, fails to teach that Port B selectively maps one of the receive lanes (on which Port B receives training sequences from Port A) to more than one of the transmit lanes (on which Port B transmits training sequence to Port A). Bunton's Port B of Figure 4 merely retransmits training sequence TS1 back to Port 1. That is, Bunton's Figure 4 fails to disclose any selective mapping of the received lanes to more than one of the transmit lanes, as recited in claim 4. Bunton's Figure 5 "shows the actual format and content of the training sets TS1 and TS2" (Bunton, column 8, lines 13-14) and Figure 6 shows lane identifiers used in various lanes. Bunton's Figures 5 and 6, however, does not disclose any selective mapping, as recited.

The Examiner, while responding to applicant's arguments, alleged that Bunton's Figure 9 discloses a mapping (Final office action dated 11/17/2006, page 3, last line). Bunton's Figure 9

shows possible link combinations when two ports with different link widths are coupled, i.e. when mixed bus widths are connected (Bunton, column 10, lines 17-26). For example, the left most column of Figure 9 shows a "1 lane transmitter 900 coupled to 1, 4, and 12 lane receivers" (Bunton, column 10, lines 31-32). The possible link combinations are between a transmitter 900 (for the left most column of the Figure) and a receiver RX, i.e. between a transmitter and a receiver of two different components. For example, the link combination may be between Bunton's Port A 400 and Port B 410 of Figure 4. To the extent Bunton's Figure 9 discloses a mapping, it is between a transmitter (e.g., transmitter 900) and a receiver of different components to support possible difference in link widths between two ports of the two different components. In contrast, claim 4 recites selectively mapping one of the receive lanes to more than one of the transmit lanes, where the transmit and the receive link interfaces are both coupled to the same memory agent through the transmit and receive link interfaces (as recited in claim 1, from which claim 4 depends).

Additionally, to the extent Bunton disclose a mapping, Bunton's Figure 9 teaches connecting one lane of the transmit port to only one lane of the receive port. In contrast, the limitation recites *the memory agent may selectively map one of the receive lanes to more than one of the transmit lanes*. Bunton does not disclose any mapping where one receive lane is coupled to *more than one* of the transmit lanes. Thus, the references do not disclose all the elements recited in claim 4, and the Examiner has not set forth a reason to modify the references to include all the limitations of claim 4. A *prima facie* case of obviousness, therefore, has not been established with respect to claim 4.

Claim 5

Claim 5 recites that *the memory agent may selectively map one or more of the first receive lanes to one or more of the second transmit lanes according to a plurality of mappings.* As discussed with respect to claim 4, Bunton fails to disclose this limitation.

Claim 7

Claim 7 recites that *the memory agent may retransmit the received training sequence with modification as the return sequence.* As disclosed in the specification, for example, the memory agent may retransmit most of the training sequence as the return sequence while modifying only

a small group within the sequence to provide identifying or status information to the memory host (substitute specification, page 36, lines 9-13).

The Examiner alleges, while rejecting claim 1, that Bunton's Figure 4 discloses that Port B may receive training sequence TS1 and retransmit it back to Port A. Bunton discloses the following with respect to Figure 4:

> "By transmitting an initial sequence of TS1 training sets 420, Port A 400 can effectively wake up Port B 410 from a disabled state to an enabled state 440. Once Port B is enabled 440, two things occur. First, Port B 410 will begin transmitting TS1 training sets back to Port A 400. Secondly, Port B 410 will check the content of the incoming TS1 training sets 420 to see if the data was received as it was sent. If there is any discrepancy, Port B 410 will correct the incoming signals so that the original content of TS1 420 is restored. At this point, Port B 410 will be trained 460 and will respond by sending the second training set, TS2 430, back to Port A 400." (Bunton, column 7, lines 48-57, underlining added).

That is, once Port B is enabled, Port B may retransmit TS1 training back to Port A, without any modification or correction. Alternatively, if there is any discrepancy, Port B corrects the incoming signal so that the original content of the incoming signal is restored. Bunton, however, does not disclose that Port B retransmits the corrected incoming signal. That is, even if the correction of the incoming signal is interpreted as modification of the received training sequence, Bunton does not disclose retransmitting back the corrected signal as the return sequence, as would be required by claim 7. Instead, after any possible correction of TS1, Bunton teaches "sending the second training set, TS2 430, back to Port A 400." (Bunton, column 7, lines 54-57, underline added). Thus, Bunton's Port B does not *retransmit the received training sequence with modification as the return sequence*, as would be required by claim 7. Because none of the cited references disclose all of the limitations of claim 7, and the Examiner has not set forth a reason to modify the references to include all the limitations, a *prima facie* case of obviousness has not been established with respect to claim 7.

CONCLUSION

Applicant requests that the rejection of claims 2-5, 7, 12 and 17 be reversed.

Customer No. 20575

Respectfully submitted,

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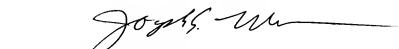

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CLAIMS APPENDIX

The claims involved in the appeal read as follows. (Note: claim 1 is not appealed, but is included here because appealed claims 2-5 and 7 depend from claim 1.)

1. (Rejected, not appealed) A memory agent comprising:

a receive link interface having a plurality of receive lanes to receive training sequences;

a transmit link interface having a plurality of transmit lanes to transmit return sequences; and

a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation.

2. (Rejected) The memory agent according to claim 1 wherein:

the receive link interface is a first receive link interface;

the transmit link interface is a first transmit link interface; and further comprising:

a second transmit link interface having a plurality of second transmit lanes; and

a second receive link interface having a plurality of second receive lanes.

3. (Rejected) The memory agent according to claim 2 wherein

the memory agent may operate in a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting return sequences received on the second receive link interface to the first transmit link interface.

4. (Rejected) The memory agent according to claim 1 wherein the memory agent may selectively map one of the receive lanes to more than one of the transmit lanes during a lane testing operation.

5. (Rejected) The memory agent according to claim 1 wherein the memory agent may selectively map one or more of the first receive lanes to one or more of the second transmit

lanes according to a plurality of mappings.

7. (Rejected) The memory agent according to claim 1 wherein the memory agent may retransmit the received training sequence with modification as the return sequence.

12. (Rejected) A memory agent comprising:

a first link interface having a plurality of first lanes; and

a second link interface having a plurality of second lanes;

wherein the memory agent may:

transmit training sequences having different mapping indicators on one or more of the plurality of first lanes;

receive return sequences on one or more of the plurality of second lanes responsive to the training sequences; and

analyze the return sequences to identify failed lanes in the plurality of first lanes and the plurality of second lanes.

17. (Rejected) The memory agent according to claim 12 wherein the memory agent may transmit electrical stress patterns in the training sequences.

EVIDENCE APPENDIX

Copies of the following references are attached:

Bunton et al. (U.S. Patent No. 6,961,347)

Li et al. (U.S. Patent No. 5,515,361)

RELATED PROCEEDINGS APPENDIX

None.